AMENDMENTS TO THE CLAIMS:

The following is a complete listing of all claims, including amendments, with a status identifier in parenthesis.

Listing of Claims

Claim 1. (Previously Amended): A method of forming a CMOS sidewall spacer, comprising the steps of:

forming a PMOS transistor gate structure on a n-type region of a semiconductor substrate;

forming a NMOS transistor gate structure on a p-type region of said semiconductor substrate;

forming initial single layer sidewall structures of similar widths adjacent to said NMOS transistor gate structure and said PMOS transistor gate structure; and

etching said initial single layer sidewall structure adjacent to said NMOS transistor gate structure such that the width of a first single layer sidewall structure adjacent to said NMOS transistor gate structure is less than the width of a second single layer sidewall structure adjacent to said PMOS transistor gate structure.

Claim 2. (Currently Amended): The method of claim 1 wherein said etching of said initial single layer sidewall structure is an [anisotropic] isotropic etch.

Claim 3. (Previously Amended): The method of claim 1 wherein said initial single layer sidewall structure is a material selected from the group consisting of silicon nitride, silicon oxide, and silicon oxynitride.

Claims 4-8 (Canceled).

Claim 9 (Currently Amended): A method of forming a CMOS sidewall spacer method comprising the steps of:

providing a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

forming a gate dielectric on said semiconductor substrate;

forming a conductive layer on said gate dielectric;

etching said conductive layer and said gate dielectric to form a first transistor gate stack with an upper surface on said semiconductor substrate of a first conductivity and a second transistor gate stack with an upper surface on said region of said semiconductor substrate of a second conductivity type;

forming LDD regions adjacent the first transistor gate stack and adjacent the second transistor gate stack;

forming a sidewall film over said semiconductor substrate;

etching said sidewall film using an anisoptropic etch such that all of said sidewall film is removed from said upper surface of said first transistor gate stack and said upper surface of said second transistor gate stack, wherein a plurality of sidewall structures of

a first width are formed adjacent to said first transistor gate stack and said second transistor gate stack;

masking said second transistor gate stack with a photoresist pattern used for source drain implantation; and

etching said sidewalls of a first width adjacent to said first transistor gate stack thereby forming sidewalls of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

Claim 10 (Original): The method of claim 9 wherein said sidewall film is silicon nitride, silicon oxide, or silicon oxynitride.

Claim 11 (Original): The method of claim 9 wherein said anisotropic etch is a plasma etch.

Claim 12 (Original): The method of claim 9 wherein said first conductivity type is p-type.

Claim 13 (Withdrawn): A CMOS integrated circuit comprising:

a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

a first transistor gate stack on said semiconductor substrate of a first conductivity;

a second transistor gate stack on said region of said semiconductor substrate of a second conductivity type;

sidewalls of a first width adjacent to said second transistor gate stack; and

sidewalls of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

Claim 14 (Withdrawn): The CMOS integrated circuit of claim 13 wherein said first conductivity type is p-type.

Claim 15 (Withdrawn): The CMOS integrated circuit of claim 13 wherein said first and second transistor gate stacks comprise a dielectric layer adjacent to a conductive layer.

Claim 16 (Withdrawn): The CMOS integrated circuit of claim 14 wherein said dielectric layer is silicon oxide, silicon oxynitride or silicon nitride.

Claim 17 (Withdrawn): The CMOS integrated circuit of claim 14 wherein said conductive layer is doped silicon or a metal.

Claim 18 (Withdrawn): The CMOS integrated circuit of claim 13 wherein said sidewalls of a first width is silicon nitride, silicon oxide, or silicon oxynitride.

Claim 19 (Withdrawn): The CMOS integrated circuit of claim 13 said sidewalls of a second width is silicon nitride, silicon oxide, or silicon oxynitride.